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PHOTOLITHOGRAPHY

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Lecture notes adapted from handout notes for

Microelectronics: An Integrated Approach

http://www.prenhall.com/howe/microelectronics/

By R. T. Howe and C.G. Sodini

Microlithography: Historical Perspective

http://www.spie.org/web/oer/february/feb97/lin.html

IC Fabrication Technology

- History:

  1958-59: J. Kilby, Texas Instruments and R. Noyce, Fairchild
  1959-70: Explosive growth in US (bipolar ICs)
  1970-85: MOS ICs introduced, RAMs, microprocessors, Japan catches up to US in volume
  1985-95: PC revolution, improved design software for complex CMOS integrated systems, US leads in micro-processors, Japan in RAMs
  1996-2000 > 10^8 devices/chip (= 1000 Mbit dRAM), US remains competitive -- even dominates -- sectors of the market; spin-offs from IC technology in MEMS (micro electro-mechanical systems) for sensing acceleration

- Key Idea: *batch fabrication* of electronic circuits

  An entire circuit, say 10^6 transistors and associated wiring -- can be made in and on top of a single silicon crystal by a series of process steps similar to printing.

  The silicon crystal is a thin disk about the size of a small dinner plate (ca. 1996) called a *wafer*. More than 100 copies of the circuit are made at the same time.

- Results:

1. Complex systems can be fabricated reliably
2. Cost per function drops as the process improves (e.g., finer printing), since the cost per processed wafer remains about the same

IC Materials and Processes

- *Polycrystalline silicon (polysilicon)*: silicon deposited from a gas at temperatures around 600 ^{o}C, made up of small crystallites (grains), so-so conductor when heavily doped with phosphorus, but can survive very high temperatures. Useful for making micromechanical structures

- *Deposited oxides*: silicon dioxide deposited from a gas at temperatures from 425 ^{o}C to 600 ^{o}C, boron and phosphorus are sometimes added to allow it to flow. These oxides are known as “CVD” oxides for “chemical vapor deposition.”

- *Metals*: aluminum is the standard “wire” for ICs and is usually deposited by “sputtering.” Tungsten (grown from a gas reaction) is sometimes used, with increasing interest in copper.

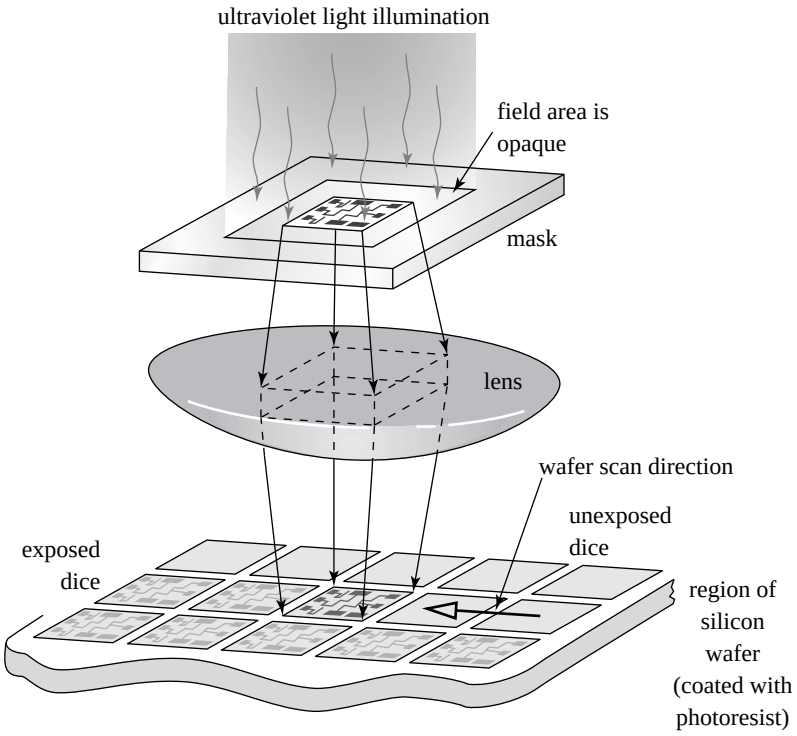
In order to make an IC, we need

1. the mask patterns (the *layout*)

2. the sequence of fabrication steps (the *process* ... or *recipe*)

Photolithography

- The essential process step: makes possible the transfer of a series of patterns onto the wafer -- all aligned to within 0.1 μm
- Process "Tool" -- *wafer stepper*



- UV-sensitive film is called *photoresist.* Regions exposed to UV dissolve in developer (for *positive* photoresist -- the type we will consider)

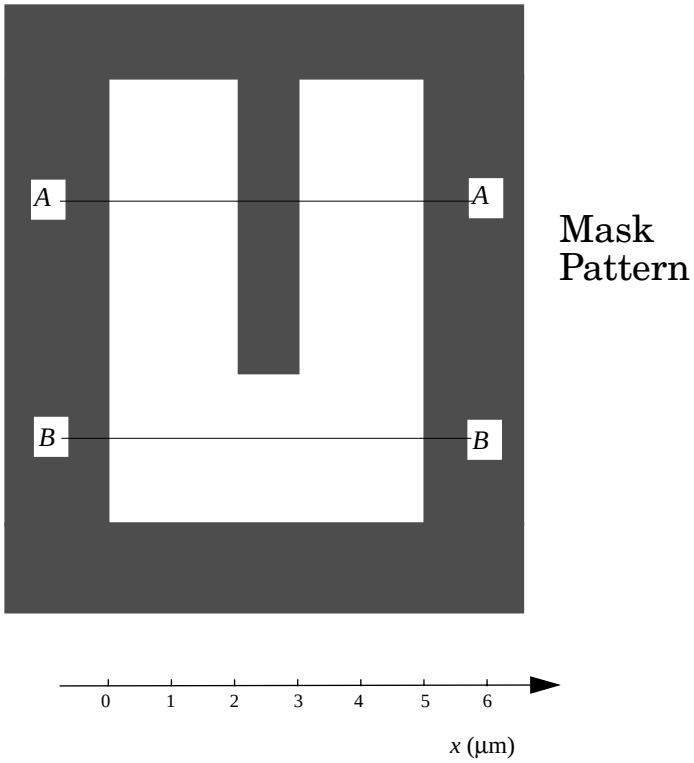
Exposure, Development, and Pattern Transfer

- Simple example of a *layout* and a *process* (or *recipe*)

  * *Layout* is the set of mask patterns for particular layers (one in this case)

  * *Process* is the sequence of fabrication steps

- Visualize by generating *cross sections* through the structure as it is built up through the process



Process Flow in Cross Sections

- Process (simplified)

  0. Clean wafer in nasty acids (HF, HNO_3, H_2SO_4, ...) --> wear gloves!

  1. Grow 500 nm of SiO_2 (by putting the wafer in a furnace with O_2

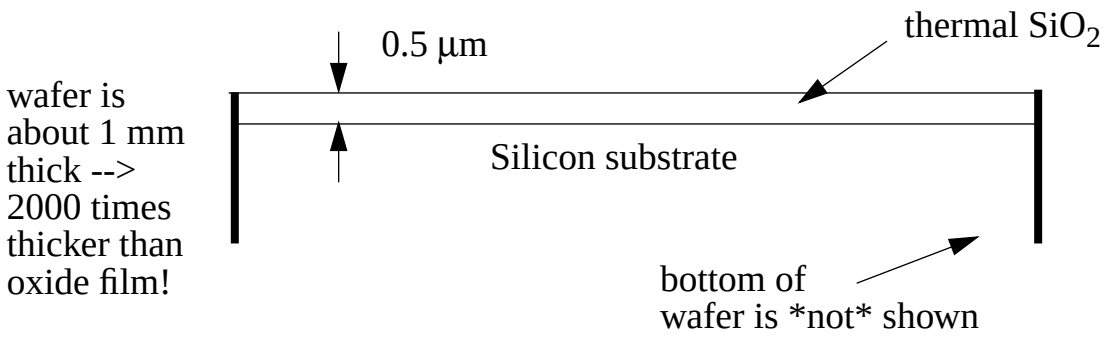
  2. Coat the wafer with 1 μm of photoresist

  3. Expose and develop the image and bake the resist to get rid solvent and to make it tougher

  4. Put wafer in a plasma etcher -- fluorine ions in plasma etch SiO_2 much faster than underlying silicon -- and etch off exposed SiO_2

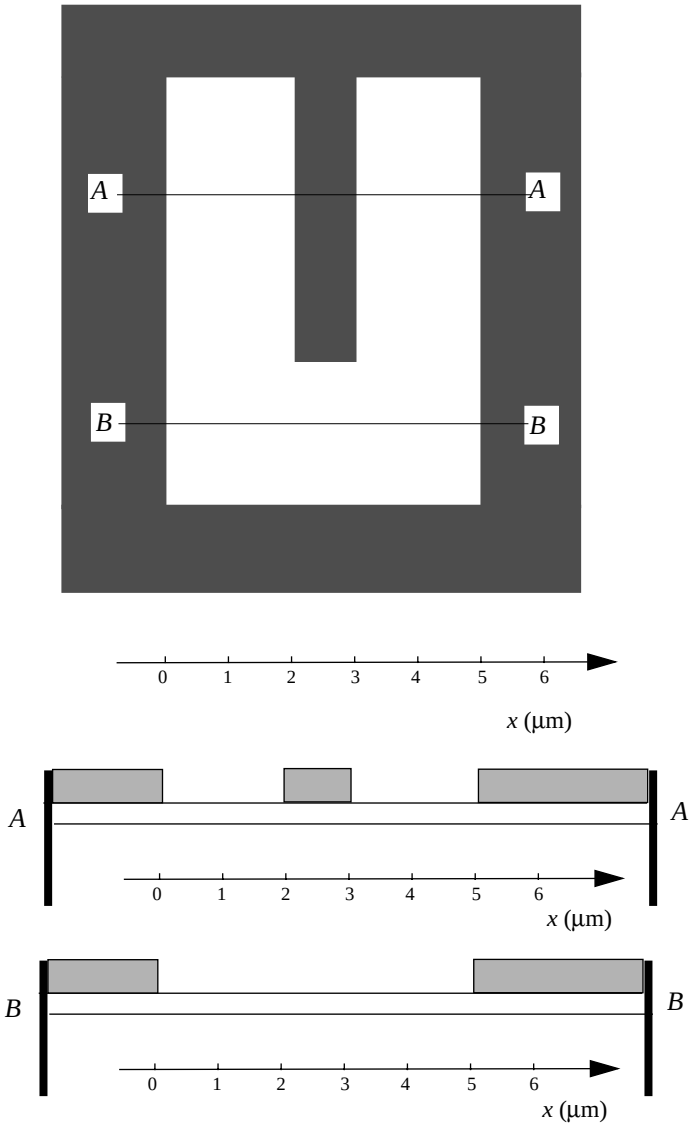
  5. Put wafer in a plasma stripper -- oxygen ions remove photoresist and leave SiO_2 untouched.

- After Step 1 (SiO_2 growth):



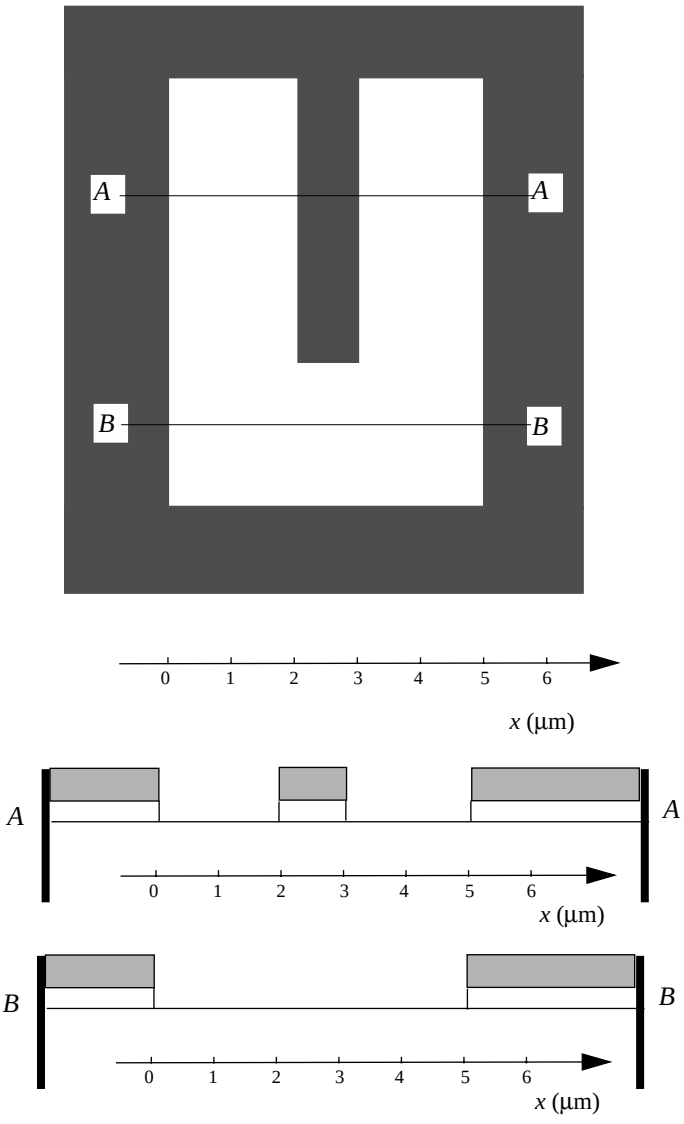
Process Flow (cont.)

- After Step 3: photoresist has been developed from clear areas of the mask



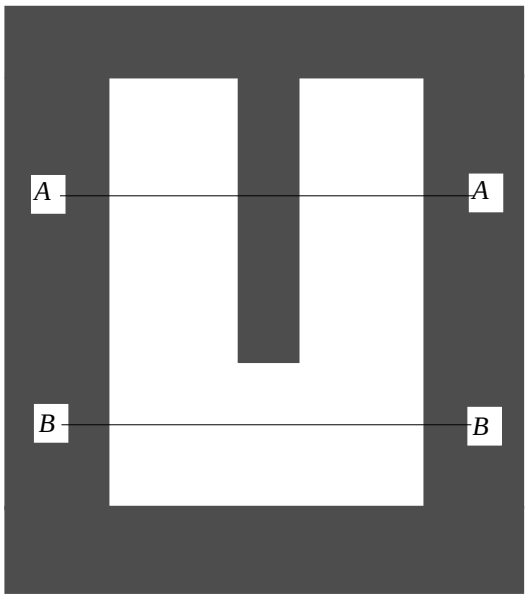
Process Flow (cont.)

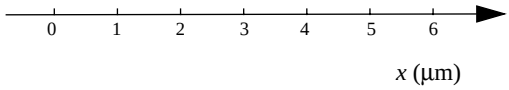
- After Step 4: oxide is etched in the fluorine plasma, without etching of the underlying silicon

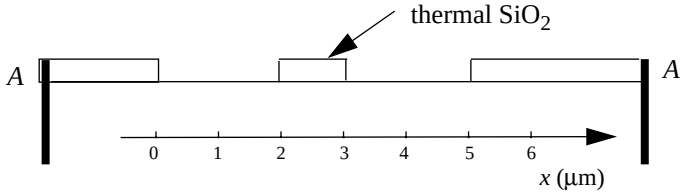


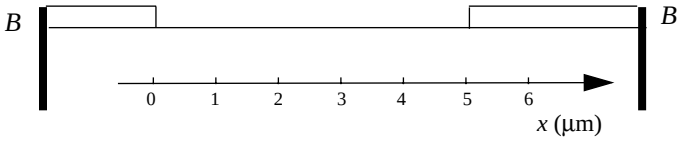
Completed Structure

- After Step 5: oxygen plasma strips (i.e., etches) the photoresist









Depicting Mask Pattern Overlays

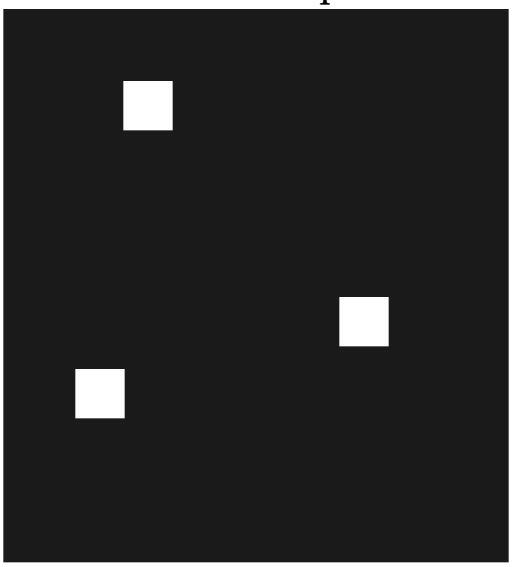
Problem: some mask plates are mostly black --> difficult to depict in the CAD layout tool since the pattern for that mask will cover underlying masks (even with high resolution color and clever "fill" patterns).

Solution: draw the negative of mostly black mask patterns in the layout editor and then label that mask carefully, so that you remember to make the inverse!

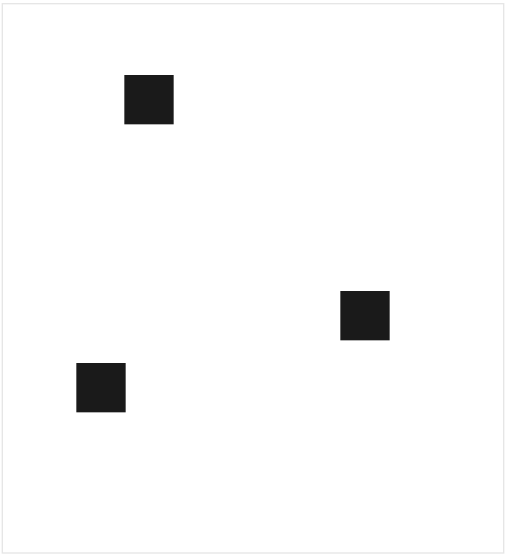
Nomenclature: "dark field" means the negative pattern is drawn
"clear field" means that the pattern is drawn

Example of a dark field mask:

actual mask plate

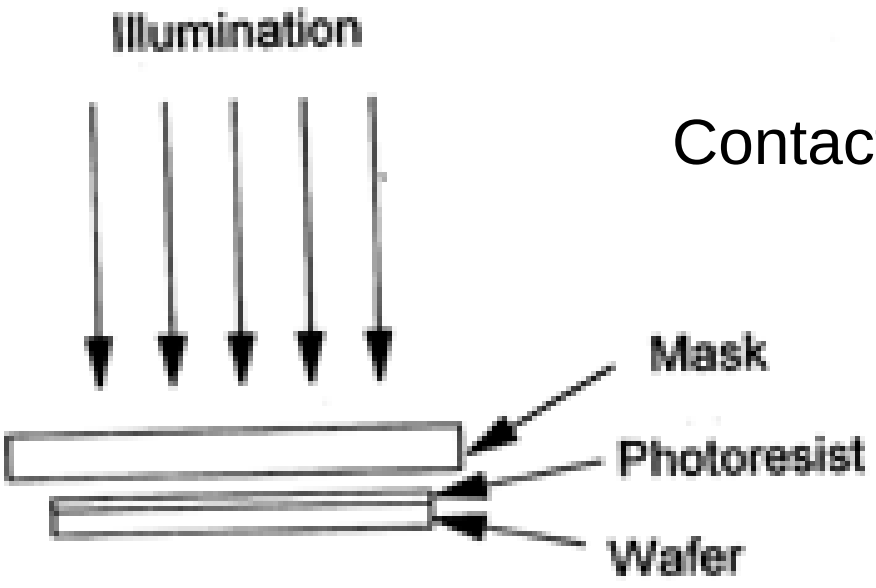


CAD layout of mask

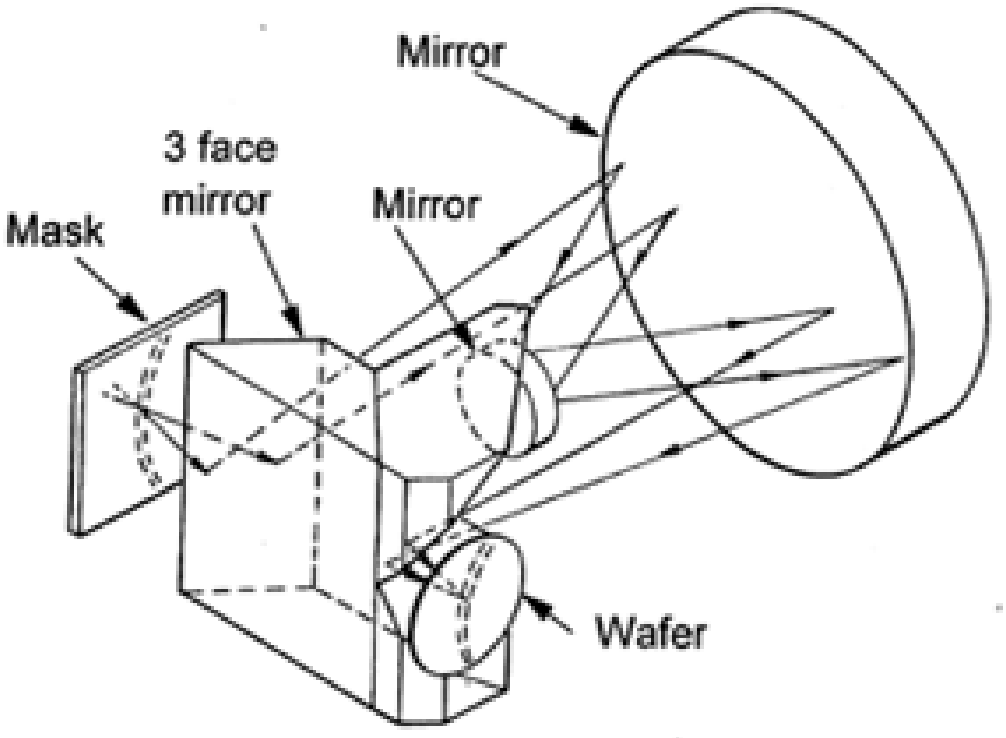


label mask pattern "dark field"

Equipment (I)

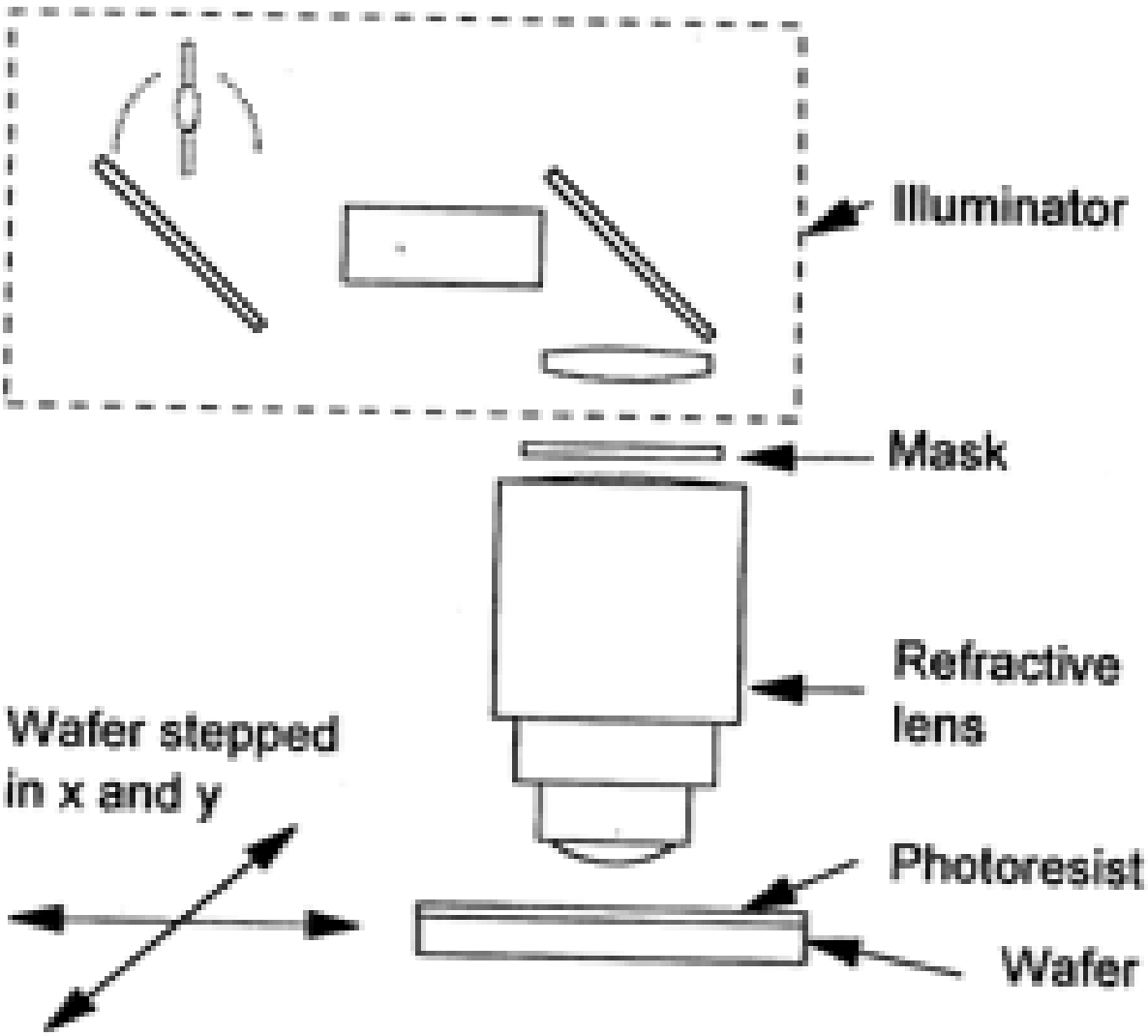


Contact (1958)



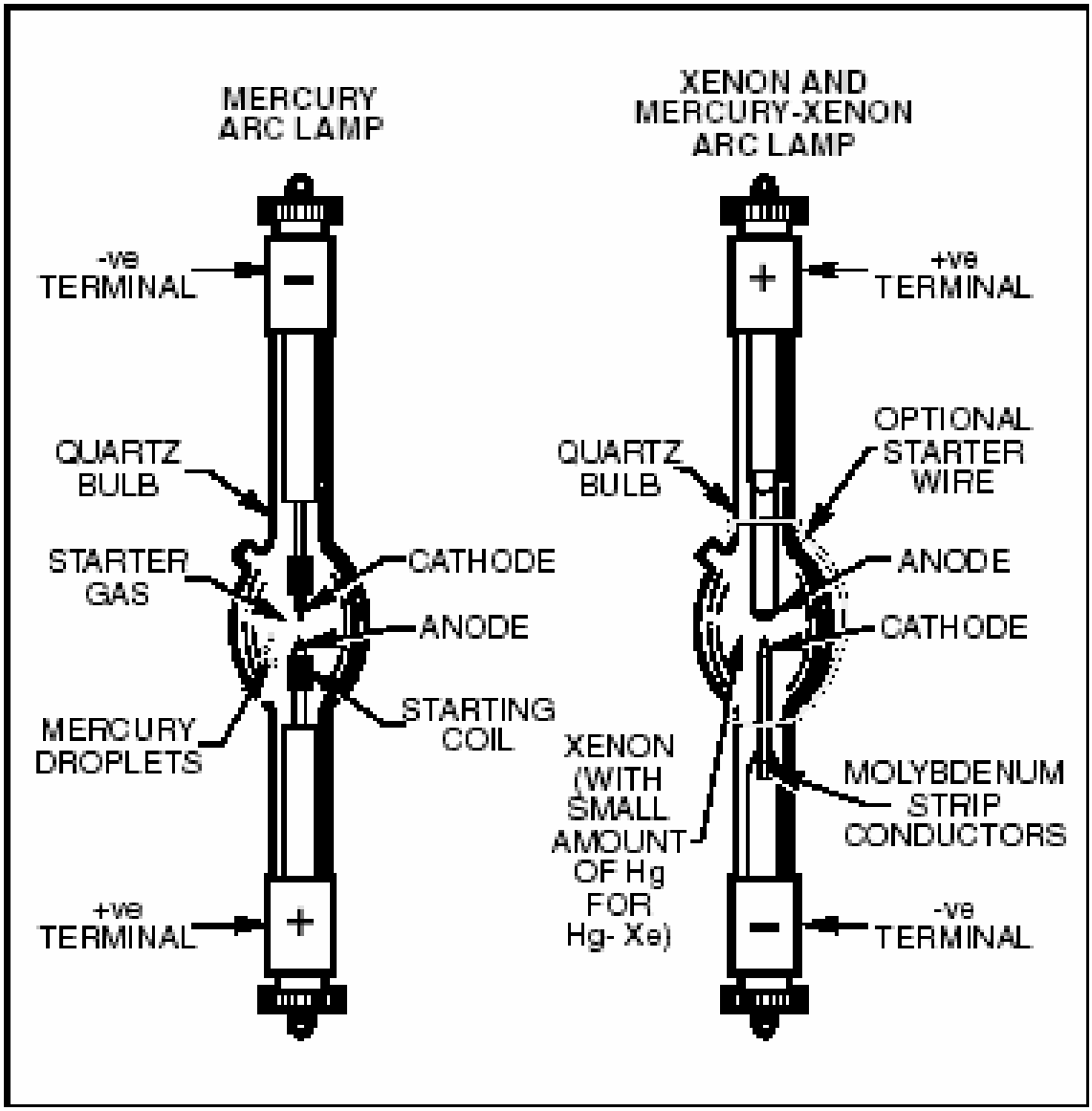
1X Projection (1974)

Equipment (II)

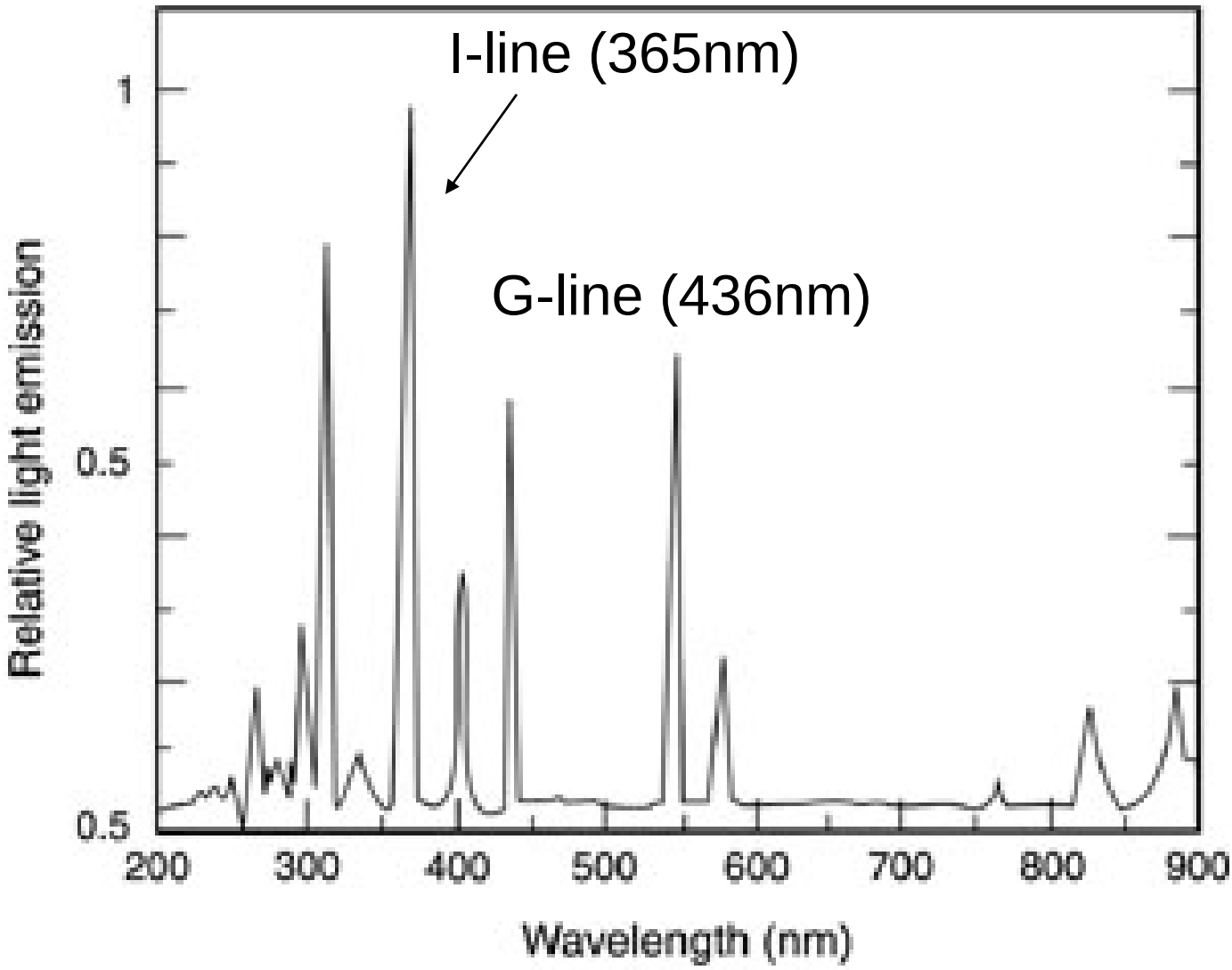


Step And Repeat (1978)

Arc Lamps


MERCURY
ARC LAMP
-ve
TERMINAL
QUARTZ
BULB
STARTER
GAS
CATHODE
ANODE
STARTING
COIL
MERCURY
DROPLETS
+ve
TERMINAL
XENON AND
MERCURY-XENON
ARC LAMP
+ve
TERMINAL
OPTIONAL
STARTER
WIRE
QUARTZ
BULB
ANODE
CATHODE
XENON
(WITH
SMALL
AMOUNT
OF Hg
FOR
Hg- Xe)
MOLYBDENUM
STRIP
CONDUCTORS
-ve
TERMINAL

Mercury (Hg) Lamp Spectrum



- Mercury lamps have limited life-time
- Must be well ventilated as they produce Ozone