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SURFACE MICROMACHINING IN SILICON ON SAPPHIRE CMOS TECHNOLOGY

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ABSTRACT

We report on the design and fabrication of surface micromachined microelectromechanical structures (MEMS) in an ultra thin silicon (UTSi) on sapphire CMOS process [Peregrine Semiconductor (PE) Silicon on Sapphire (SOS) process] [1]. This is the first demonstration of surface micromachined MEMS structures in a CMOS process fabricated on a sapphire substrate.

1. INTRODUCTION

Integration of MEMS devices with their measurement and control electronics on a single chip has long been a goal of MEMS research. The Analog Devices iMEMS [2] process is a BiCMOS technology that incorporates low stress polysilicon layers for mechanical structures. Another approach to highly integrated micromechanical elements and electronics is the postprocessing of standard CMOS to release MEMS structures. Simple mechanical structures as well as passive elements with reduced parasitics (capacitors and inductors) have been reported using bulk micromachining in CMOS[3]-[4]. Alternatively, mechanical elements can be fabricated as composite structures comprised of the various metal interconnect and insulating oxide layers available in standard CMOS technologies, often referred to as CMOS-MEMS. The pioneering work in G. Fedder's group at Carnegie Mellon has demonstrated that CMOS-MEMS is a viable single chip solution for building sensors, actuators and their supporting electronics[5], [6], [7] in a number of different commercially available bulk CMOS technologies.

The Peregrine Semiconductor SOS-CMOS process is a 0.5 micron technology with, 100 nm thin silicon layer, 3 metal interconnection layers and 1 or 2 polysilicon layers. There are two variants of this technology available for fabrication, FA and FC. The FC process utilized in this demonstration has a 3 micron thick top metal layer normally used for making high quality inductors and capacitors in radio frequency circuits.

In this paper we report on surface micromachining of mechanical structures in the Peregriine SOS-CMOS process. The polysilicon gate and the thin silicon layers act as sacrificial release layers. The MEMS structures employ composite beams formed from the 3 metal layers and the oxides between them in the Peregrine FC SOS-CMOS technology.

There are a number of advantages when using the SOS process [8],[9]: Optical transparency, low power, high speed and radiation hardness. In addition, the UTSi SOS technology provides devices with lower parasitic capacitances than standard CMOS technologies and offers the designer six types of MOSFETs, as compared to the two types in most other bulk CMOS technologies. The fully depleted devices with their lower threshold, higher normalized transconductance, and reduced parasitics yield high performance analog blocks. High performance analog circuitry can be used to accurately control, measure, and output the information content of the MEMS elements avoiding the complicated steps of hybrid integration.

2. DESIGN OF SOS-CMOS MEMS STRUCTURES

Working with Peregrine Semiconductor we have modified slightly the design rules to allow for the fabrication of the MEMS structures. The first test chip was fabricated in the Fall of 2003 through Peregrine Semiconductor directly (fig. 1). The prototype chip has test structures for evaluating

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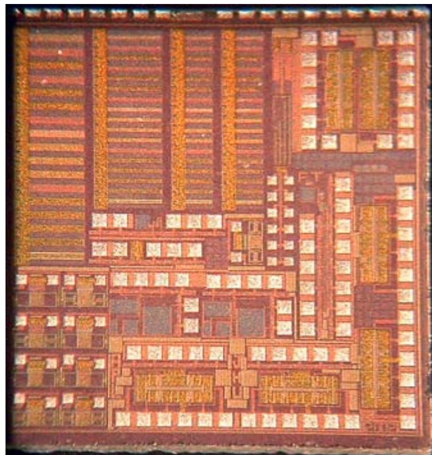

Fig. 1. Photomicrograph of the SOS-CMOS MEMS test die

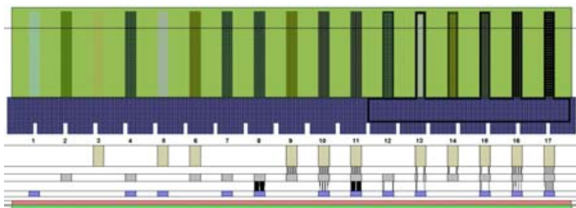

Fig. 2. Physical layout and cross sections of the cantilever test beams.

the feasibility of surface micromachining and enabling basic material, mechanical and electrostatic characterization.

The first and most basic MEMS structures are four sets of cantilever beams. Each set of 17 beams is constructed from different combinations of metal layers and the vias connecting the metal layers (fig. 2). Each set of 17 beams varies in a single dimension. This allows for the determination of the Young's Modulus of each composite beam as well as for each individual layer by determining the beams resonant frequency[10]. The residual stress for each beam can be determined from the radius of curvature following release.

At a second level of complexity, we include simple suspended mass and comb drive structures. These devices have the same proof mass which is composed of all 3 metal layers, the mass also has etch holes to help with release. The mass is supported by one of two spring systems, both spring systems use all 3 metal layers. One spring is a simple beam spring. It has an anchor which spans the width of the proof mass and has two beams which run from the anchor to the

Fig. 3. Photomicrograph of fully released cantilever beams

corners of the proof mass. The other spring is a folded spring. It has an anchor located near the mass, the anchor has two thin beams running away from the mass and into a thicker free moving cross bar. At the ends of the cross bar beams run back towards the proof mass and make contact at the corners. The last component of these structures are the comb drives.

There are two variations of the comb drives and two different sizes. There are long 30 micron fingers in one drive and shorter 10 micron fingers in the second. One comb drive uses only metal 1 and 2 the second uses all 3 metal layers. This is because the design rules for metal 3 are not as tight as for the first two metals and we wanted to examine the tradeoff between thicker fingers versus more closely packed fingers. These structures will help to characterize the performance of the anchors, the flexibility of the springs and lastly which comb drive setup yields the most electrostatic potential.

The most complex MEMS structure on the first test chip is a xylophone bar magnetometer. These magnetometers have been designed to enable comparison with well characterized polysilicon MUMPS and CMOS-MEMS devices previously designed in our group [11]. There are a few variations of the magnetometer design which yield different resonant frequencies and provide the ability to use the vibrating bar as a mixer.

The magnetometers will also show if the reduced parasitic capacitances provided by the SOS process will improve capacitive sensing of mechanical motion by eliminating the stray capacitance to the bulk. The xylophone bar tests the limits of the release steps by pushing the minimum etch hole gap down to 1.2 microns.

3. POST PROCESSING FOR MEMS RELEASE

The post-processing steps were formulated to minimize their effect on the characteristics of the CMOS electronics. The test chip includes transistors, amplifiers and photodiodes. The devices will be characterized to determine whether the post-processing steps for MEMS adversely affect the electronic devices. We post process die received from PE in two steps. First we perform an etching step through all layers to reach the substrate. Metal-3 is the mask for this step that defines the structures in the plane. The second step is a release

step to free the structures from the substrate.

Structures definition: The etch is performed using a Trion Phantom inductively coupled plasma (ICP) reactive ion etcher (RIE). One common problem seen with this type of etching is the formation of RIE residue, commonly known as grass. Two potential causes of grass formation are; re-sputtering of exposed metals such as the metal mask or metal surfaces in the RIE reactor chamber and polymer formation due to the plasma etch chemistry. Another obstacle is undercutting and erosion of the metal mask. If the vertical to horizontal etch rate is not sufficient and the metal mask is undercut the composite MEMS devices delaminate. Metal mask undercutting is also the reason that a dry etch is preferred to a wet chemical etch with HF.

We have encountered severe RIE residue problems. Metal-1 lines where completely hidden underneath a layer of grass. Using energy dispersive spectroscopy(EDS) we determined the grass was primarily composed of Al, F, and O_2. We performed 14 etch trials, which varied every etch parameter. After replacing chamber parts, that where composed of anodized aluminum, with graphite parts the problem was solved. We can now routinely etch the oxide layers without leaving RIE grass or degrading the metal mask. Depending on etch parameters total etch time through approximately 10 microns of oxide is between 50 and 100 minutes.

Structures release: This second step removes the polysilicon and silicon sacrificial layers. This lateral etch undercuts all the MEMS devices and frees them from the substrate. This etch is performed using a pulsed XeF_2 vapor system. The pulsed system sublimates XeF_2 crystals for 1 minute, then pauses for 1 minute while the reactants are used. The chamber is then flushed and the process is repeated. The total etch time for this step is 40 minutes or 20 etching cycles.

Since only sacrificial polysilicon and silicon are exposed, over-etching is not an issue with this step. All electronics are encapsulated in oxide which the XeF_2 vapor can not penetrate. We have successfully undercut and released cantilever beams without etch holes that spanned 200 microns on their shortest side. All devices have been successfully released.

4. DISCUSSION

The SOS-CMOS MEMS structures have been successfully released, demonstrating that it is possible to fabricate electromechanical structures in this technology.

As expected residual stresses cause significant curling in the large cantilever beams (fig. 3). The radius of curvature is being measured so the residual stress levels can be calculated. We use a Veeco white light optical profilometer (fig. 4). Smaller structures such as interdigitated capacitive fingers do not show curling this is illustrated in the magnetometer structure(fig. 5) where both the main beam and the capacitive sense fingers remain flat. This is important because when short beams curl it makes design of capacitive sense and electrostatic actuation structures more difficult and area intensive.

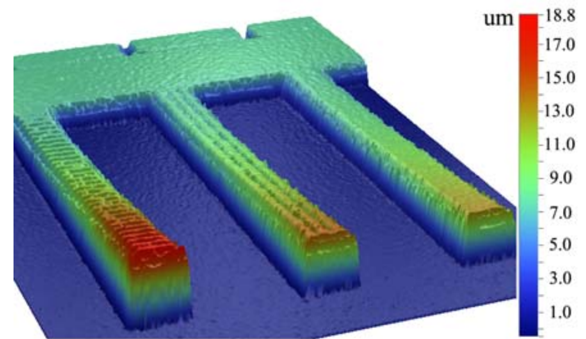

Fig. 4. Optical profile data beams 15 through 17

Fig. 5. SEM photographs of entire (top) and close-up (bottom) of magnetometer

A laser induced thermal excitation is used to determine the resonant frequency for each of the 17 cantilever beams (fig. 6). The thermal excitation setup uses one laser to heat the beam while another laser with a different wavelength is reflected off the MEMS device and into a bi-cell photodetector. When the MEMS device moves it deflects the second laser beam which is detected in the bi-cell, at resonant frequency the amplitude of the deflection is maximized. The resonant frequency and Q factor are determined through this method. We have calculated Young's Modulus for beams 15 and 16 to be 60.6 GPa and 61.1 GPa respectively. This is comparable to published results of the individual Al and $Si0_2$ materials[10].

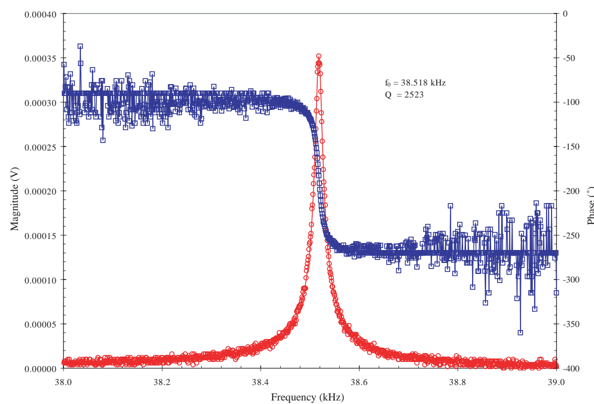

Fig. 6. Resonance peak from thermally excited cantilever beam number 16

Characterization of the simple suspended mass structure is underway. The cantilever beams could be characterized before the RIE grass issue was solved, the suspended mass could not because the grass hinders the electrostatic actuation of the device. The suspended mass has been moved with a probe tip proving full release of the structure.

The magnetometer has proved difficult to test. In previous designs thermal excitation was possible much like with the cantilever beams, but due to the large etch holes in the main beam of the device it is difficult to get good signal in the beam deflection system. Also the RIE grass hinders the devices motion, testing of clean devices is underway.

5. CONCLUSIONS

We have successfully demonstrated the design and fabrication of MEMS structures in the Peregrine Semiconductor silicon on sapphire CMOS technology. Initial measurements of Young's modulus for the composite structures are in good agreement with published results. Further testing of all devices is underway. The initial results are encouraging and suggest that further investigation of this approach to CMOS-MEMS is worth pursuing.

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